XL1326

Dual CAN FD and Six-Channel USART Industrial Connectivity Controller

2 x CAN FD | 6 x USART | 6 x TNOW | USB 2.0 Full-Speed

LQFP48 | 7 mm x 7 mm | 0.50 mm pitch

Production Datasheet

Version V1.05 | August 2026

XL1326 Datasheet Revision History

Table 1. Datasheet revision history

Version	Date	Revision History
V0.10P	August 2026	Initial engineering release.
V1.00	August 2026	Production release; host protocol, TNOW outputs, RS-422 support and complete package drawing added.
V1.01	August 2026	Pin-configuration visibility revision; TNOW1 through TNOW6 labels added to the pin-configuration drawing.
V1.02	August 2026	Product-neutral reference design, USB identity, fixed 8.000 MHz main clock and package mechanical drawing revision.
V1.03	August 2026	Unified Xilume logo placement; clarified the fixed eight-port host model; aligned HELLO and GET_INFO with production firmware.
V1.04	August 2026	Production firmware V7.2.2; corrected pin-1 orientation; normalized HELLO reserved fields and CAN FD bit-rate replies; clarified system-powered USB integration; added latch-up and controlled packaging/compliance guidance.
V1.05	August 2026	Documentation-only layout revision: aligned the header mark and increased reference-design symbol clearances. No electrical, protocol, pin or firmware change.

Product Status

PRODUCTION DATA: This document defines the production customer interface for XL1326. Use the complete orderable code when placing an order.

Scope

This datasheet defines the customer-visible pin functions, host interface, USB protocol, electrical limits, application requirements and LQFP48 package of XL1326. The device is supplied as a fixed-function industrial connectivity controller.

Important Use Limitations

- External CAN, RS-232, RS-422 and RS-485 line transceivers are required; the corresponding XL1326 pins are logic-level signals.
- IC-level ESD ratings do not replace connector-level ESD, EFT, surge, isolation or EMC protection in the finished product.
- Pins marked NC shall remain unconnected. RSV1 and RSV2 require the fixed bias specified in this document.
- The device is not intended for life-support, flight-critical, nuclear-control or other safety-critical use unless separately qualified in writing by Xilume.

Terms and Conventions

Table 2. Terms and conventions

Term	Meaning
USART1...USART6	Six independent asynchronous communication channels.
TNOW1...TNOW6	Automatic transmit-direction outputs corresponding to USART1...USART6.
RSV	Reserved connection; apply only the specified fixed bias.
NC	No Connect; leave unconnected.
XILUME-MUX-V1	USB Bulk transport framing used by the host interface.

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1. General Description

XL1326 combines two independent CAN FD controllers, six independent USART controllers, six automatic transmit-direction outputs and one USB 2.0 Full-Speed device interface in a 48-pin LQFP package. The fixed-function architecture is intended for general communication equipment, industrial computers, robots, automation systems and test equipment.

All six USART channels expose fixed TX, RX and corresponding TNOW signals. External transceivers select RS-232, full-duplex RS-422, two-wire RS-485 or four-wire RS-485 electrical operation without changing the USB logical-channel assignment.

Only the fixed communication and support signals documented in this datasheet are customer accessible.

1.1 Applications and Features

- Two CAN FD channels: up to 1 Mbit/s nominal and 8 Mbit/s data phase.
- Classical CAN data frames and CAN FD data frames with 11-bit or 29-bit identifiers, subject to the Protocol Version 1 limits in Section 6.5.
- Six USART channels configurable from 300 bit/s to 3,000,000 bit/s.
- Six active-high TNOW outputs for automatic two-wire RS-485 direction control.
- USB 2.0 Full-Speed vendor-specific interface with one Bulk OUT and one Bulk IN endpoint.
- Eight logical host channels: CAN FD 1, CAN FD 2 and USART1 through USART6.
- 2.4 V to 3.6 V operating supply; complete USB electrical limits at 3.0 V to 3.6 V; -40 °C to +105 °C ambient range.
- LQFP48 package, 7 mm x 7 mm body, 0.50 mm lead pitch.

1.2 Device Boundary

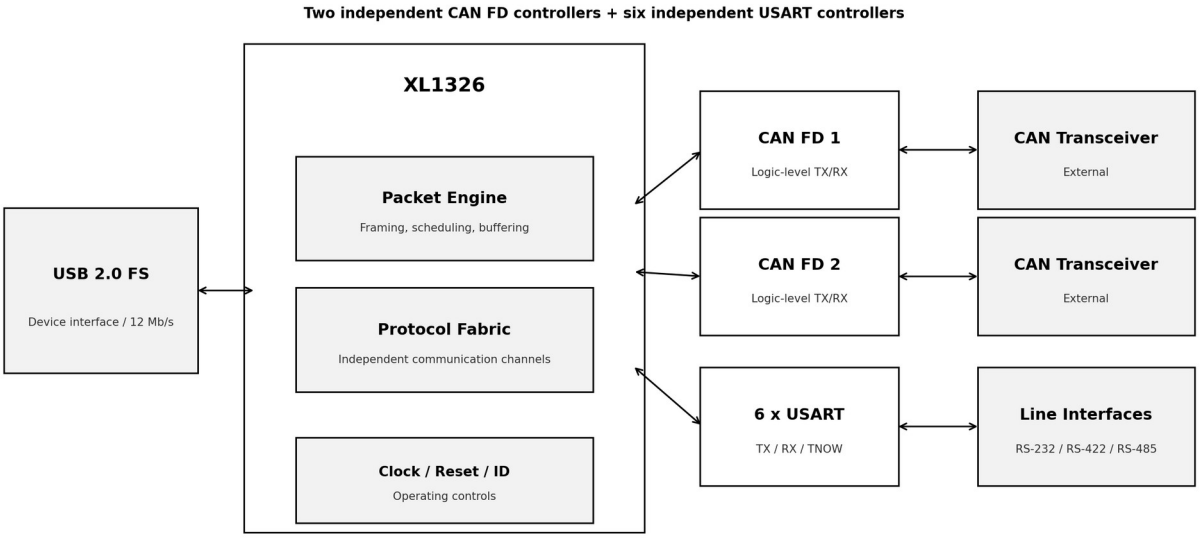
Table 3. Device boundary

Integrated in XL1326	Implemented externally
Two CAN FD controllers and host transport	CAN FD transceivers, termination, isolation and protection
Six USART controllers and six TNOW outputs	RS-232, RS-422 or RS-485 transceivers and connector protection
USB 2.0 Full-Speed physical interface	USB connector, optional system-level protection and board power implementation
Clock, reset, device identity and channel scheduling	Application connectors, indicators, power conversion and enclosure

2. Functional Architecture

2.1 Functional Block Diagram

Figure 1. XL1326 functional block diagram.



2.2 Interface Summary

Table 4. Interface summary

Interface	Count	Maximum rate	Function
CAN FD	2	1 Mbit/s nominal; 8 Mbit/s data	Independent CAN data-frame channels
USART	6	3,000,000 bit/s per channel	Independent asynchronous TX and RX
TNOW	6	Functional timing	Automatic active-high transmit direction
USB device	1	12 Mbit/s line rate	Aggregate host command and data transport
Main clock	1	8.000 MHz crystal or resonator	Communication timing reference
Auxiliary clock	1	32.768 kHz typical	Optional low-frequency time base

2.3 Logic-Level Boundary

CAN1_TX/CAN1_RX and CAN2_TX/CAN2_RX connect only to logic-side pins of external CAN FD transceivers. USARTn_TX, USARTn_RX and TNOWn are logic-level signals referenced to VSS. They shall not be connected directly to CANH/CANL, RS-232 cable pins or RS-422/RS-485 differential pairs.

3. Pin Configuration

Figure 2. XL1326 LQFP48 pin configuration (top view).

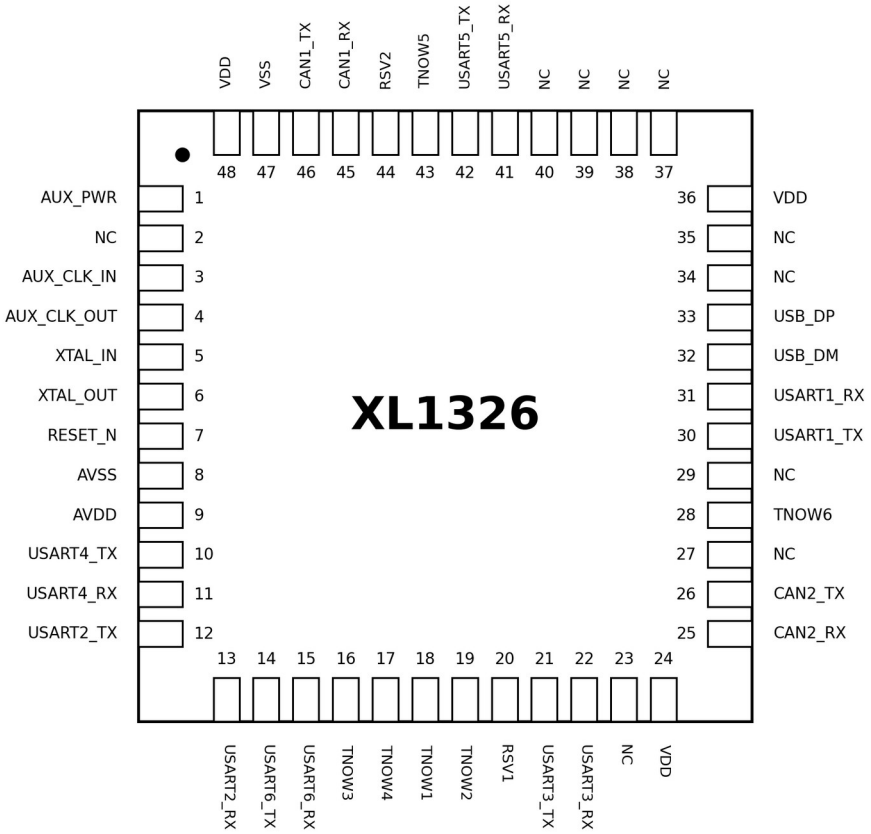


Table 5. Pin-type legend

Type	Meaning
P	Power or ground
I	Digital input
O	Digital output
I/O	Bidirectional interface
A	Oscillator or analog connection
RSV	Reserved connection; apply only the specified fixed bias
NC	No Connect; leave unconnected

The molded index mark identifies the pin-1 corner. Figure 2 is a top view; confirm footprint orientation before assembly.

4. Pin Description

4.1 Pins 1 to 24

Table 6. Pin description - pins 1 to 24

Pin No.	Pin Name	Type	Description
1	AUX_PWR	P	Auxiliary supply. Tie to VDD when an independent auxiliary supply is not used.
2	NC	NC	No Connect. Leave unconnected.
3	AUX_CLK_IN	A	Optional low-frequency crystal or clock input.
4	AUX_CLK_OUT	A	Optional low-frequency crystal output.
5	XTAL_IN	A	8.000 MHz main-crystal input.
6	XTAL_OUT	A	8.000 MHz main-crystal output.
7	RESET_N	I	Active-low device reset input.
8	AVSS	P	Analog ground; connect to VSS.
9	AVDD	P	Analog supply; connect to VDD and decouple locally.
10	USART4_TX	O	USART channel 4 transmit output.
11	USART4_RX	I	USART channel 4 receive input.
12	USART2_TX	O	USART channel 2 transmit output.
13	USART2_RX	I	USART channel 2 receive input.
14	USART6_TX	O	USART channel 6 transmit output.
15	USART6_RX	I	USART channel 6 receive input.
16	TNOW3	O	Automatic transmit-direction output for USART3, active high. Low selects receive/idle; high selects transmit. Asserted before the first start bit and held high until the final stop bit is complete.
17	TNOW4	O	Automatic transmit-direction output for USART4, active high. Low selects receive/idle; high selects transmit. Asserted before the first start bit and held high until the final stop bit is complete.
18	TNOW1	O	Automatic transmit-direction output for USART1, active high. Low selects receive/idle; high selects transmit. Asserted before the first start bit and held high until the final stop bit is complete.
19	TNOW2	O	Automatic transmit-direction output for USART2, active high. Low selects receive/idle; high selects transmit. Asserted before the first start bit and held high until the final stop bit is complete.
20	RSV1	RSV	Connect to VSS through a dedicated 10 kΩ resistor. Do not connect to any other signal.
21	USART3_TX	O	USART channel 3 transmit output.
22	USART3_RX	I	USART channel 3 receive input.
23	NC	NC	No Connect. Leave unconnected.
24	VDD	P	Digital supply. Connect every VDD pin.

4. Pin Description (continued)

4.2 Pins 25 to 48

Table 7. Pin description - pins 25 to 48

Pin No.	Pin Name	Type	Description
25	CAN2_RX	I	CAN channel 2 receive input from an external transceiver.
26	CAN2_TX	O	CAN channel 2 transmit output to an external transceiver.
27	NC	NC	No Connect. Leave unconnected.
28	TNOW6	O	Automatic transmit-direction output for USART6, active high. Low selects receive/idle; high selects transmit. Asserted before the first start bit and held high until the final stop bit is complete.
29	NC	NC	No Connect. Leave unconnected.
30	USART1_TX	O	USART channel 1 transmit output.
31	USART1_RX	I	USART channel 1 receive input.
32	USB_DM	I/O	USB Full-Speed D- line.
33	USB_DP	I/O	USB Full-Speed D+ line.
34	NC	NC	No Connect. Leave unconnected.
35	NC	NC	No Connect. Leave unconnected.
36	VDD	P	Digital supply. Connect every VDD pin.
37	NC	NC	No Connect. Leave unconnected.
38	NC	NC	No Connect. Leave unconnected.
39	NC	NC	No Connect. Leave unconnected.
40	NC	NC	No Connect. Leave unconnected.
41	USART5_RX	I	USART channel 5 receive input.
42	USART5_TX	O	USART channel 5 transmit output.
43	TNOW5	O	Automatic transmit-direction output for USART5, active high. Low selects receive/idle; high selects transmit. Asserted before the first start bit and held high until the final stop bit is complete.
44	RSV2	RSV	Connect to VSS through a dedicated 10 kΩ resistor. Do not connect to any other signal.
45	CAN1_RX	I	CAN channel 1 receive input from an external transceiver.
46	CAN1_TX	O	CAN channel 1 transmit output to an external transceiver.
47	VSS	P	Digital ground reference.
48	VDD	P	Digital supply. Connect every VDD pin.

NC pins: 2, 23, 27, 29, 34, 35, 37, 38, 39 and 40. Do not connect these package lands to traces, test points, pull resistors or external logic.

RSV1 (pin 20) and RSV2 (pin 44) each require an independent 10 kΩ resistor to VSS.

5. Functional Description

5.1 CAN FD Controllers

Table 8. CAN FD capabilities

Capability	Production support
Channels	Two independent CAN FD channels
Frame formats	Classical CAN data frames and CAN FD data frames
Identifier range	11-bit standard and 29-bit extended, subject to Section 6.5
Payload	0 to 8 bytes Classical CAN; 0 to 64 bytes CAN FD
Bit rate	10 kbit/s to 1 Mbit/s nominal; up to 8 Mbit/s data phase
BRS	Supported
External physical layer	Required CAN FD transceiver

5.2 USART and TNOW

Table 9. USART and TNOW assignment

Channel	TX pin	RX pin	Direction output	Pin
USART1	30	31	TNOW1	18
USART2	12	13	TNOW2	19
USART3	21	22	TNOW3	16
USART4	10	11	TNOW4	17
USART5	42	41	TNOW5	43
USART6	14	15	TNOW6	28

TNOWn is a push-pull active-high output. It changes high before the first start bit and returns low only after the final stop bit is complete. No fixed nanosecond lead or hold interval is specified. TNOW outputs shall not be externally driven or connected together.

5.3 External Physical Layers

Table 10. External physical-layer options

Standard	Topology	External implementation	TNOW use
RS-232	Single-ended, full duplex	RS-232 transceiver	Leave TNOW open
RS-422	Two differential pairs, full duplex	RS-422 transceiver	Leave TNOW open
RS-485 2-wire	One differential pair, half duplex	RS-485 transceiver with DE and /RE	Connect TNOW to DE and /RE
RS-485 4-wire	Two differential pairs, full duplex	Full-duplex RS-485 transceiver	Normally leave open; optional DE control

5. Functional Description (continued)

5.4 USB Device Interface

The host interface is a USB 2.0 Full-Speed vendor-specific device. It is not a USB CDC ACM interface. A compatible Xilume host driver or a host implementation of Section 6 is required.

The production host model always contains eight logical ports. The Xilume Windows driver exposes eight independent virtual COM child devices. Driver ports 1 and 2 carry CAN FD 1 and CAN FD 2; ports 3 through 8 carry USART1 through USART6. Windows-assigned COM numbers are dynamic. The Xilume Linux driver maps logical channels 0 and 1 to two SocketCAN interfaces and channels 2 through 7 to six TTY interfaces. The logical-channel mapping in Table 15 does not change.

Table 11. USB device descriptor

Descriptor field	Value
USB specification	2.00
Speed	Full-Speed
Device class / subclass / protocol	0x00 / 0x00 / 0x00; interface-defined
EP0 maximum packet	64 bytes
VID	0x2E3C
PID	0x5740
bcdDevice	0x0722
Configurations	1
Language ID	0x0409

Table 12. USB string descriptors

Index	Descriptor	Value
1	Manufacturer	Xilume
2	Product	XL1326
3	Device identifier	12 uppercase hexadecimal characters, unique per device
4	Configuration	XL1326
5	Interface	XL1326 Host Interface

Table 13. USB configuration and interface

Field	Value
Configuration total length	32 bytes
Configuration value	1
Interfaces	1
bmAttributes	0xC0, self-powered
Declared maximum bus current	100 mA
Interface / alternate setting	0 / 0
Interface class / subclass / protocol	0xFF / 0x00 / 0x00

Table 14. USB endpoint assignment

Endpoint	Direction	Transfer type	Maximum packet
0x01	Host to XL1326	Bulk OUT	64 bytes
0x81	XL1326 to host	Bulk IN	64 bytes

No device qualifier, other-speed configuration or remote-wakeup capability is advertised. Host data is carried through the two Bulk endpoints.

bcdDevice is encoded as BCD 7.22 (0x0722), while HELLO reports semantic device revision 7.2.2. Datasheet V1.05 specifies production firmware V7.2.2.

6. Host Interface and USB Protocol

6.1 Logical Channels and Framing

Figure 3. USB transport and logical-channel map.

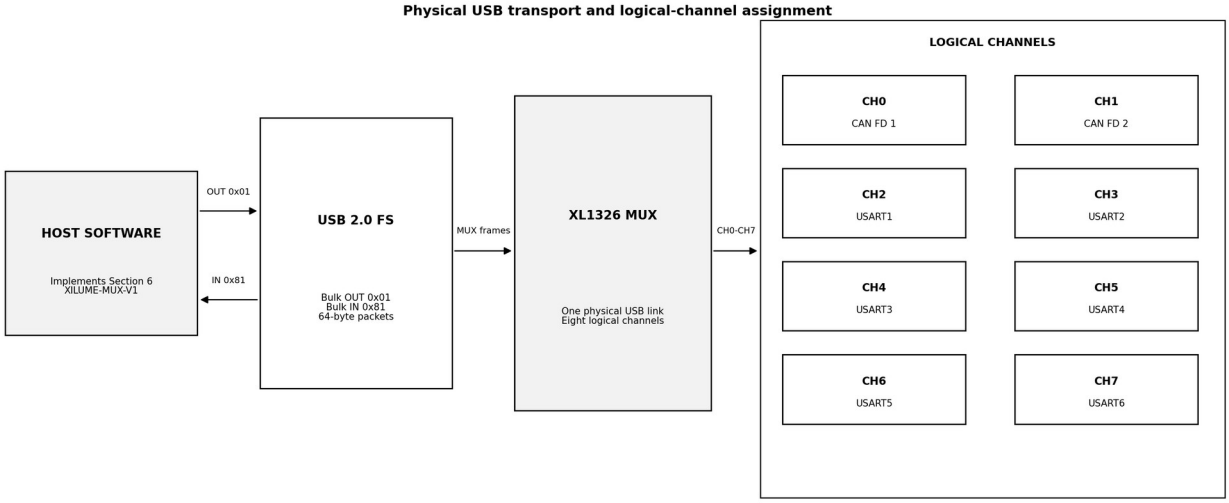


Table 15. Logical channel assignment

Logical channel	Driver port	Function	Payload interpretation
0	1	CAN FD 1	CAN ASCII command and response stream
1	2	CAN FD 2	CAN ASCII command and response stream
2	3	USART1	Raw USART byte stream
3	4	USART2	Raw USART byte stream
4	5	USART3	Raw USART byte stream
5	6	USART4	Raw USART byte stream
6	7	USART5	Raw USART byte stream
7	8	USART6	Raw USART byte stream
0xFF	-	Device control	HELLO transaction only

Driver port numbers are stable 1-based labels; Windows COM numbers are assigned dynamically and need not match them.

All six USART logical channels use the same raw byte-stream protocol with external RS-232, full-duplex RS-422 or RS-485 transceivers. RS-422 requires no separate MUX mode or capability bit.

Figure 4. XILUME-MUX-V1 frame layout.

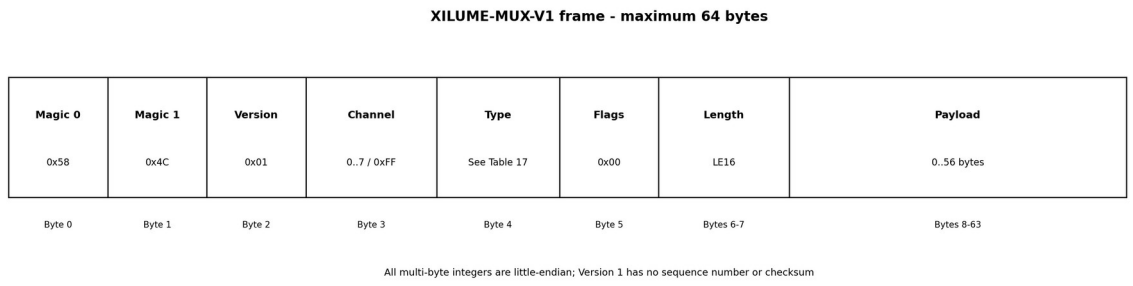


Table 16. XILUME-MUX-V1 header

Offset	Size	Field	Definition
0	1	Magic 0	0x58
1	1	Magic 1	0x4C
2	1	Protocol version	0x01
3	1	Logical channel	0x00-0x07 or 0xFF for HELLO
4	1	Frame type	See Table 17
5	1	Flags	Shall be 0x00 in Version 1
6	2	Payload length	0x0000-0x0038, little-endian

6. Host Interface and USB Protocol (continued)

Table 17. XILUME-MUX-V1 frame types

Type	Name	Direction	Purpose
0x01	DATA	Both	CAN ASCII stream or raw USART bytes
0x02	CONFIG	Host to XL1326	Configure USART parameters
0x03	CONTROL	Host to XL1326	Open, close, purge or break
0x04	STATUS_REQUEST	Host to XL1326	Request USART status
0x7E	HELLO	Both	Protocol negotiation
0x80	ACK	XL1326 to host	Request acknowledgement
0x81	STATUS	XL1326 to host	USART status response
0xFF	ERROR	XL1326 to host	Request or framing error

6.2 HELLO Transaction

After claiming the USB interface, the host sends a zero-length HELLO frame on logical channel 0xFF. Applications shall not open logical channels until the HELLO response has been validated.

Table 18. HELLO response payload

Offset	Field	Value
0	Protocol version	1
1	Logical channel count	8
2	CAN channel count	2
3	USART channel count	6
4	RS-485 / TNOW capable count	6
5	Reserved	0x00
6	Physical USB transport count	1
7	Maximum MUX payload	56
8	Device revision major	7
9	Device revision minor	2
10	Device revision patch	2
11	Capability flags	0x03

Table 19. HELLO capability flags

Bit	Meaning
0	CAN ASCII stream supported
1	CAN transmit confirmation supported
7:2	Reserved

HELLO payload offset 5 is reserved and returns 0x00. Hosts shall ignore reserved response bytes and unknown capability bits so later compatible revisions can extend the response. External RS-232, RS-422 and RS-485 line-interface choices do not change the logical-channel protocol.

HELLO example

```
Host:  58 4C 01 FF 7E 00 00 00
Device: 58 4C 01 FF 7E 00 0C 00  01 08 02 06 06 00 01 38 07 02 02 03
```

6. Host Interface and USB Protocol (continued)

6.3 USART Transactions

Logical channels 2 through 7 carry raw USART bytes. Successful DATA, CONFIG and CONTROL requests receive an ACK. Multi-byte values in all payloads are little-endian.

Table 20. MUX ACK payload

Offset	Size	Field	Definition
0	1	Original request type	Type being acknowledged
1	1	Status	0 success; 2 partial or busy
2	2	Bytes accepted	Number of payload bytes accepted

Table 21. USART CONFIG payload

Offset	Size	Field	Valid values
0	4	Baud rate	300 to 3,000,000 bit/s
4	1	Data bits	7 or 8
5	1	Parity	0 none; 1 odd; 2 even
6	1	Stop bits	0 one; 1 one-and-a-half; 2 two
7	1	Reserved	Send 0x00

Default configuration is 115200 bit/s, 8 data bits, no parity and one stop bit. Mark/space parity, 5/6 data bits and RTS/CTS flow control are not supported.

For a successful CONFIG request, Bytes accepted is 8. For CONTROL, it is the CONTROL payload length. STATUS_REQUEST is valid only on channels 2 through 7, has zero payload bytes and returns a type-0x81 STATUS frame with a 26-byte payload.

Table 22. USART CONTROL operations

Operation	Payload	Meaning
0x01	[0x01, open]	Set open state; zero closed, non-zero open
0x02	[0x02, mask]	Purge queues; bit 0 RX, bit 1 TX
0x03	[0x03]	Send break when the external transmitter is continuously enabled

Table 23. USART STATUS payload

Offset	Size	Field
0	4	Baud rate
4	1	Data bits
5	1	Parity
6	1	Stop bits
7	1	Open state
8	1	Transmitting state
9	1	Reserved
10	2	RX bytes queued
12	2	TX bytes queued
14	4	RX overflow count
18	4	TX overflow count
22	4	USART error count

6. Host Interface and USB Protocol (continued)

MUX Error Response

ERROR payload format is [request_type, error_code].

Table 24. MUX error codes

Code	Meaning
1	Invalid logical channel
2	Reserved
3	Invalid target channel or payload length
4	Unsupported USART format
5	Unknown CONTROL operation
6	Status unavailable
7	Unknown frame type
8	Invalid alignment, magic or protocol version
9	Invalid, excessive or incomplete payload length
10	Trailing bytes after the final complete frame

USART Transfer Examples

```
CONFIG USART1 115200 8-N-1
Host: 58 4C 01 02 02 00 08 00  00 C2 01 00 08 00 00 00
ACK:  58 4C 01 02 80 00 04 00  02 00 08 00
```

```
USART4 DATA 11 22 33
Host: 58 4C 01 05 01 00 03 00  11 22 33
ACK:  58 4C 01 05 80 00 04 00  01 00 03 00
```

```
USART1 STATUS REQUEST
Host:   58 4C 01 02 04 00 00 00
Device: 58 4C 01 02 81 00 1A 00  00 C2 01 00 08 00 00 00 00 00 00 00 00 00
        00 00 00 00 00 00 00 00 00 00 00 00
```

The STATUS example shows the state immediately after initialization with the channel closed and all queues and counters at zero.

TNOW BREAK LIMIT: SEND BREAK does not assert TNOW. It is valid only when the external transmitter is continuously enabled and is not transmitted through a two-wire RS-485 interface controlled by TNOW.

6. Host Interface and USB Protocol (continued)

6.4 CAN ASCII Protocol

Logical channels 0 and 1 carry case-sensitive, line-oriented ASCII commands inside DATA payloads. Commands end with CR, LF or CRLF. A command may span multiple DATA frames; the device retains the partial line until a terminator is received.

Table 25. CAN ASCII commands

Command	Syntax	Function
PING	PING	Connection test
GET_INFO	GET_INFO	Return model, revision and capabilities
GET_STATUS	GET_STATUS	Return CAN status and error counters
GET_BITRATE	GET_BITRATE [CAN1|CAN2]	Return nominal and data bit rate
GET_TIMING	GET_TIMING [CAN1|CAN2]	Return complete active timing
SET_FD_BITRATE	SET_FD_BITRATE CANx nominal data	Change nominal and data bit rate
SET_TIMING	SET_TIMING CANx nominal NSP NSJW data DSP DSJW SSP	Configure calculated timing
SET_TIMING_RAW	SET_TIMING_RAW CANx DIV NBTS1 NBTS2 NSJW DBTS1 DBTS2 DSJW SSPOFF	Configure raw timing
RESET_CAN	RESET_CAN [CAN1|CAN2]	Reset the selected CAN channel
TX	TX id length [data...]	Transmit Classical CAN data frame
TX2	TX2 id length [data...]	CAN2 legacy alias; CAN2 channel only
TXFD	TXFD CANx id length BRS|NOBRS [data...]	Transmit CAN FD data frame

CAN Identifier and Payload Rules

- CANx shall match the logical channel carrying the command: channel 0 is CAN1 and channel 1 is CAN2.
- Identifier range is 0x00000000 to 0x1FFFFFFF; decimal and 0x-prefixed hexadecimal forms are accepted.
- Classical CAN length is 0 to 8 bytes. CAN FD lengths are 0 to 8, 12, 16, 20, 24, 32, 48 or 64 bytes.
- Bit-rate tokens accept decimal bit/s or K/M suffixes, for example 500K or 2M.
- Data-byte tokens are hexadecimal. BRS enables data-phase rate switching; NOBRS disables it.

```
CAN1 PING
Host:   58 4C 01 00 01 00 06 00  50 49 4E 47 0D 0A
Device: 58 4C 01 00 01 00 0B 00  50 4F 4E 47 20 43 41 4E 31 0D 0A
```

6. Host Interface and USB Protocol (continued)

Table 26. CAN timing limits

Parameter	Range / rule
Nominal bit rate	10,000 to 1,000,000 bit/s
Data bit rate	10,000 to 8,000,000 bit/s
Nominal/data sample point	50.0% to 95.0%
NSJW / DSJW	AUTO or 1 to 128 TQ
SSP	AUTO or 0 to 255 TQ
DIV	1 to 32
NBTS1	2 to 513
NBTS2	1 to 128
DBTS1	2 to 257
DBTS2	1 to 128
Active timing reference	160,000,000 Hz, reported by GET_TIMING
Default	500 kbit/s nominal, 2 Mbit/s data, 75.0% / 75.0% sample points

NSJW shall not exceed NBTS2 and DSJW shall not exceed DBTS2. SSP=AUTO or a non-zero manual SSPOFF requires DIV 1 or 2. Requested bit rates must be exactly realizable from the 160 MHz timing reference using legal segment values; otherwise XL1326 returns ERR UNSUPPORTED_TIMING. Timing changes remain active until device reset or power removal.

Table 27. CAN response and receive formats

Operation or frame	ASCII format
PING response	PONG CAN1 or PONG CAN2
GET_BITRATE / SET_FD_BITRATE	OK FD_BITRATE CANx NOMINAL=<decimal> DATA=<decimal>
RESET_CAN success	OK RESET_CAN CANx
TX success	OK TX_DONE CANx
TXFD success	OK TXFD_DONE CANx
CAN1 Classical receive	RX 0xID length [data...]
CAN2 Classical receive	RX2 0xID length [data...]
CAN FD receive	RXFD CANx 0xID length BRS|NOBRS [data...]

OK TX_DONE and OK TXFD_DONE confirm completion of the bus transmission, not queue admission. Every response and received-frame line ends in CRLF.

GET_BITRATE and a successful SET_FD_BITRATE both return NOMINAL and DATA as unsigned decimal bit/s values without K or M suffixes.

Detailed CAN response templates

```
GET_INFO response:
OK INFO MODEL=XL1326 FW=7.2.2 USB_LANES=1 VIRTUAL_COMS=8 PORT=CANx
CHANNELS=8 PROTOCOL=XILUME-MUX-V1 LEGACY_TEXT=YES
CLASSIC=YES FD=YES BRS=YES TIMING=REGISTER_READBACK TXCONFIRM=YES
GET_STATUS response:
OK STATUS PORT=CANx ACTIVE=YES FD=YES TEC=n REC=n BUSOFF=n
KOER=n EPASS=n EWARN=n TPE=n TPA=n RESET=n STBY=n TSTAT=current/final
GET_TIMING response; also returned after successful SET_TIMING or SET_TIMING_RAW:
OK TIMING CANx CLOCK=n DIV=n NOMINAL=n NSP=n.n NBTS1=n NBTS2=n NSJW=n
DATA=n DSP=n.n DBTS1=n DBTS2=n DSJW=n SSP=AUTO|MANUAL SSPOFF=n
```

Response templates are visually wrapped for layout; no CR or LF occurs before the final CRLF.

In GET_INFO, CANx is CAN1 on logical channel 0 and CAN2 on logical channel 1.

CAN Error Strings

```
Every entry below is prefixed by ERR and followed by CRLF.
UNKNOWN_CMD / LINE_TOO_LONG / FORMAT / ID / DLC / DATA / CHANNEL
COM_CHANNEL_MISMATCH / BRS / PARAMETER / SSP / UNSUPPORTED_TIMING
DIV / NBTS1 / NBTS2 / NSJW / DBTS1 / DBTS2 / DSJW
UNSUPPORTED_BITRATE / RESET_CAN_FAILED
{TX|TXFD}_{BUSY|FAILED|TIMEOUT} CANx TEC=n REC=n BUSOFF=n KOER=n TSTAT=n
```

6. Host Interface and USB Protocol (continued)

6.5 Host Rules, Limitations and Examples

KOER values: 0 no error; 1 bit; 2 form; 3 stuff; 4 acknowledgement; 5 CRC; 6 other; 7 protocol-CRC/reserved. TSTAT values: 0 idle; 1 ongoing; 2 arbitration lost; 3 transmitted; 4 aborted; 5 disturbed/error; 6 rejected/malformed.

GET_STATUS abbreviations: TEC transmit error counter; REC receive error counter; BUSOFF bus-off active; EPASS error-passive state; EWARN error-warning state; TPE primary-transmit enable; TPA primary-transmit abort; RESET reset state; STBY transceiver standby state.

Table 28. Protocol Version 1 limitations

Item	Protocol Version 1 definition
Classical remote frames	Not represented
Extended-ID indication	No explicit IDE field; IDs above 0x7FF are interpreted as extended
Low-number extended ID	An extended frame with numeric ID 0x7FF or below cannot be distinguished from a standard frame
CAN FD ESI	Not encoded in the ASCII receive format
USART flow control	No RTS/CTS fields
MUX integrity	No sequence number or checksum; relies on USB Bulk transport
Aggregate throughput	All eight channels share one USB Full-Speed link; simultaneous saturation is not guaranteed
Two-wire RS-485 break	SEND BREAK is not driven through TNOW-controlled two-wire RS-485
Host implementation	Platform-specific drivers and APIs are documented separately

Host Transfer Rules

- A complete MUX frame shall not be divided across USB OUT transfers. One frame per transfer is recommended.
- Multiple complete frames may share one transfer when the combined length does not exceed 64 bytes.
- CAN and USART streams may continue across multiple DATA frames and shall be reassembled independently per logical channel.
- The host shall continuously service endpoint 0x81 and serialize writes to endpoint 0x01.
- Because ACK has no transaction identifier, do not leave multiple acknowledgement-dependent requests outstanding on the same logical channel.

Host software shall implement the transport, channel mapping and command rules in Section 6. Platform-specific driver packages, installation behavior and operating-system support are documented separately from this device datasheet.

CAN FD command example

```
Example CAN FD command stream on logical channel 0:
TXFD CAN1 0x123 12 BRS 00 01 02 03 04 05 06 07 08 09 0A 0B\r\n
```

7. Clock, Reset and Power

7.1 Supply Connections

Table 29. Supply connections

Supply	Pins	Operating range	Connection guidance
VDD	24, 36, 48	2.4 V to 3.6 V	Connect all pins; place 100 nF at each pin and add 4.7 µF bulk capacitance nearby
VSS	47	0 V	Digital ground reference
AVDD	9	Same potential as VDD	Connect to VDD; decouple with 100 nF and 1 µF
AVSS	8	Same potential as VSS	Connect directly to the ground plane
AUX_PWR	1	1.62 V to 3.6 V	Auxiliary domain only; VDD is still required for main operation. Tie to VDD when no independent auxiliary supply is used

7.2 Clock Inputs

Table 30. Clock inputs

Clock	Pins	Range / use
Main crystal	XTAL_IN pin 5; XTAL_OUT pin 6	8.000 MHz crystal or resonator
Auxiliary clock	AUX_CLK_IN pin 3; AUX_CLK_OUT pin 4	32.768 kHz crystal when required

7.3 Reset and Defined External States

RESET_N (pin 7) is active low. Keep the trace short and away from switching nodes. An external supervisor may be used when required by the system ramp or brownout environment. A 100 nF capacitor to VSS may be fitted when compatible with the selected supervisor.

RSV1 and RSV2 each require 10 kΩ to VSS. A 10 kΩ pull-down on every common TNOW-to-DE-and-/RE node is recommended so the external RS-485 transmitter remains disabled during power sequencing. TNOW becomes low after device initialization and remains low in receive/idle state.

7.4 Decoupling

Place a 100 nF ceramic capacitor at each VDD pin, one 100 nF capacitor at AUX_PWR, and 100 nF plus 1 µF at AVDD. Add a 4.7 µF bulk capacitor close to the device supply entry. Minimize every capacitor-to-pin-to-ground current loop.

8. Electrical Characteristics

Unless otherwise stated, limits apply over the recommended VDD and ambient-temperature range. Values inherited from the physical silicon and LQFP48 package are listed only where they affect a customer-visible XL1326 function. Application-dependent supply current and aggregate communication performance require XL1326 operating-state characterization and are not inferred from unrelated internal operating modes.

8.1 Absolute Maximum Ratings

Table 31. Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	Unit
VDDx-VSS	Main and analog supply voltage	-0.3	4.0	V
VAUX-VSS	Auxiliary supply voltage	-0.3	4.0	V
VIN	Voltage on customer-visible signal pins	VSS - 0.3	4.0	V
|Delta VDDx|	Difference between supply pins	-	50	mV
|VSSx-VSS|	Difference between ground pins	-	50	mV
IVDD	Total current into supply pins	-	150	mA
IVSS	Total current out of ground pins	-	150	mA
IIO-SINK	Output sink current per output/control pin	-	25	mA
IIO-SOURCE	Output source current per output/control pin	-25	-	mA
TSTG	Storage temperature	-60	+150	°C
TJ	Maximum junction temperature	-	125	°C

Absolute maximum ratings are stress limits only. Functional operation at these limits is not implied.

8.2 Recommended Operating Conditions

Table 32. Recommended operating conditions

Symbol	Parameter	Minimum	Nominal	Maximum	Unit
VDD	Digital and analog supply	2.4	3.3	3.6	V
AUX_PWR	Auxiliary-domain supply; does not power the main device	1.62	3.3	3.6	V
VDD	Supply for complete USB electrical limits	3.0	3.3	3.6	V
fXTAL	Main external crystal or resonator	-	8.000	-	MHz
TA	Ambient operating temperature	-40	-	+105	°C

8.3 Power-on and Reset Characteristics

Table 33. Power-on and reset characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
tVDD-RISE	VDD rise rate	0	-	unbounded	ms/V
tVDD-FALL	VDD fall rate	20	-	unbounded	µs/V
VPOR	Power-on reset threshold	1.73	2.06	2.40	V
VLVR	Low-voltage reset threshold	1.62	1.88	2.16	V
VLVR-HYS	Low-voltage reset hysteresis	-	180	-	mV
tRESET	Reset release delay after VDD exceeds VPOR	-	830	-	µs

8. Electrical Characteristics (continued)

8.4 Digital and USB Interface Characteristics

Table 34. Digital and USB interface characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VIL	Digital input-low voltage	USART_RX and CAN_RX; excludes RESET_N, clock and USB	-0.3	-	0.28 VDD + 0.1	V
VIH	Digital input-high voltage	USART_RX and CAN_RX; excludes RESET_N, clock and USB	0.31 VDD + 0.8	-	VDD + 0.3	V
VIL-RST	RESET_N input-low voltage	VDD = 2.4 V to 3.6 V	-0.3	-	0.72	V
VIH-RST	RESET_N input-high voltage	VDD = 2.4 V to 3.6 V	2.0	-	VDD + 0.3	V
RPU-RST	RESET_N internal pull-up	-	30	40	50	kΩ
tRST-REJ	RESET_N low pulse that may be rejected	-	-	-	40	µs
tRST-MIN	Guaranteed RESET_N low pulse width	-	80	-	-	µs
VOL	Digital output-low voltage	XL1326 production drive setting; IOL = 4 mA; VDD = 2.7 V to 3.6 V	-	-	0.4	V
VOH	Digital output-high voltage	XL1326 production drive setting; IOH = -4 mA; VDD = 2.7 V to 3.6 V	VDD - 0.4	-	-	V
VOL-LV	Digital output-low voltage	XL1326 production drive setting; IOL = 2 mA; VDD = 2.4 V to <2.7 V	-	-	0.4	V
VOH-LV	Digital output-high voltage	XL1326 production drive setting; IOH = -2 mA; VDD = 2.4 V to <2.7 V	VDD - 0.4	-	-	V
tSTARTUP	USB transceiver startup	By design	-	-	1	µs
VDI	USB differential input sensitivity	USB_DP / USB_DM	0.2	-	-	V
VCM	USB differential common-mode range	Includes VDI range	0.8	-	2.5	V
VSE	USB single-ended receiver threshold	-	1.3	-	2.0	V
VOL-USB	USB static output-low voltage	RL = 1.24 kΩ to 3.6 V	-	-	0.3	V
VOH-USB	USB static output-high voltage	RL = 15 kΩ to VSS	2.8	-	3.6	V
RPU	USB_DP internal pull-up, idle	VIN = VSS	0.97	1.24	1.58	kΩ
RPU	USB_DP internal pull-up, receive	VIN = VSS	1.66	2.26	3.09	kΩ
tr	USB rise time	CL <= 50 pF	4	-	20	ns
tf	USB fall time	CL <= 50 pF	4	-	20	ns
trfm	USB rise/fall-time matching	tr / tf	90	-	110	%
VCRS	USB output crossover voltage	-	1.3	-	2.0	V
VESD-HBM	Human-body-model ESD	All pins	±2000	-	-	V
VESD-CDM	Charged-device-model ESD	All pins	±1000	-	-	V
ILATCH	Latch-up immunity	JESD78F, Class II/A	±200	-	-	mA

USB operation is functional from 2.7 V, but the complete USB electrical limits are specified only from 3.0 V to 3.6 V. ESD and selected timing values are design-qualified and are not individually measured on every shipped unit. XL1326 supply-current limits will be published only after characterization in defined USB, CAN and USART operating states.

8.5 System Qualification Boundary

Connector-level surge, EFT, ESD, radiated or conducted immunity, isolation and regulatory compliance depend on the external circuitry, PCB and complete product construction.

9. Application Information

9.1 Minimum Connection Checklist

1. Connect VDD pins 24, 36 and 48 and provide local decoupling at each pin.
2. Connect AVDD to VDD, AVSS to VSS and AUX_PWR to VDD when no independent auxiliary supply is used.
3. Connect RSV1 pin 20 and RSV2 pin 44 individually to VSS through 10 kΩ.
4. Connect a qualified 8.000 MHz crystal or resonator between XTAL_IN and XTAL_OUT. Other main-clock frequencies are not supported by the XL1326 production configuration.
5. Route USB_DP and USB_DM as a controlled-impedance differential pair; add connector-side protection only when required by the end-system compliance target.
6. Use external CAN FD transceivers and place termination only at physical bus ends.
7. Use external RS-232, RS-422 or RS-485 transceivers; connect TNOW only where transmit-direction control is required.
8. Leave NC pins 2, 23, 27, 29, 34, 35, 37, 38, 39 and 40 open.

9.2 USB Layout

Route USB_DP and USB_DM as a short, length-matched 90 Ω differential pair. Avoid stubs, test pads and plane discontinuities. Optional 0 Ω to 22 Ω series-tuning footprints may be placed near XL1326. If the end-system compliance target requires connector-side protection, select a suitably low-capacitance device and place it at the connector. In the default system-powered 3.3 V topology, keep USB connected for the entire period that XL1326 is powered, and apply or remove VDD and the USB connection together with the complete system. Designs with independently controlled power domains or USB hot-plug while XL1326 remains powered require system-level VBUS presence detection and connection management; this is outside the default reference design.

9.3 CAN and USART Physical Layers

Choose transceivers rated for the required voltage, temperature, common-mode range and data rate. For an isolated interface, maintain creepage and clearance across the complete PCB, connector and enclosure path. Do not connect outputs from multiple optional receive transceivers directly together; select one receive path using assembly options, a switch or a tri-state device.

9.4 Validation

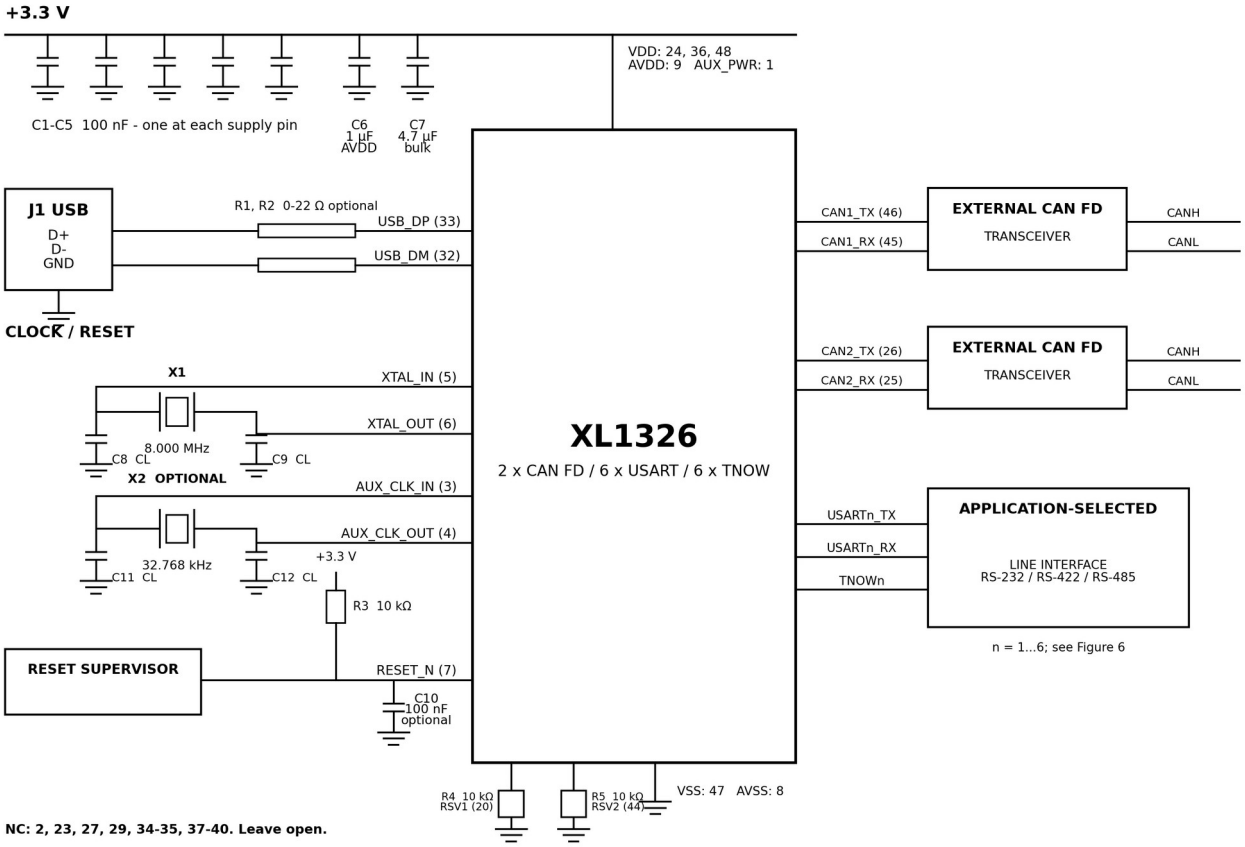
- Exercise both CAN FD channels and all six USART channels concurrently under the expected host load.
- Verify TNOW polarity and turnaround with the selected RS-485 transceiver.
- Verify USB enumeration, suspend/resume recovery, reset recovery and brownout behavior.
- Validate temperature, EMC and transient immunity on the complete product.

9. Application Information (continued)

9.5 Reference Design

Figure 5 is a generic 3.3 V minimum connection example. It shows the device power, clocks, reset, reserved-pin bias and logic-side connections. Protection, isolation, connectors and external physical-layer devices are selected for the target system and are not fixed by XL1326.

Figure 5. Generic XL1326 minimum connection example.



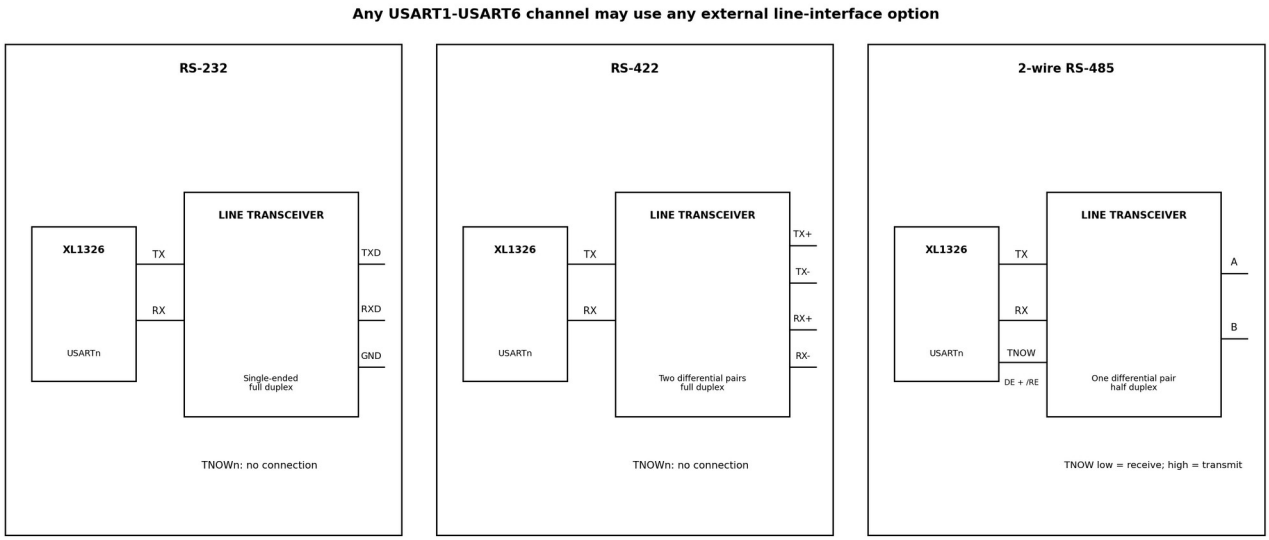
For two-wire RS-485, connect USARTn_TX to DI, USARTn_RX to RO and TNOWn to the common DE and /RE node. Add 10 kΩ from this node to the transceiver-side ground so receive mode is selected during power sequencing. For isolated designs, use a non-inverting TNOW isolation path with a defined low output.

Fit CAN and RS-485 termination only at physical bus ends. The USB series resistors are tuning footprints; select final values after signal-integrity validation.

9. Application Information (continued)

9.6 USART Physical-Layer Options

Figure 6. USART physical-layer connection options.



TNOW Connection Rules

- Two-wire RS-485: connect TNOW to the transceiver DE and /RE common node; add a 10 kΩ pull-down.
- Full-duplex RS-422: keep the driver and receiver continuously enabled and leave TNOW open.
- Four-wire RS-485: normally keep DE high and /RE low; TNOW may control DE only when transmitter tri-state operation is required.
- RS-232: connect only USART TX/RX to the logic side of the transceiver and leave TNOW open.
- TNOW is an output. Do not externally drive it and do not connect different TNOW outputs together.

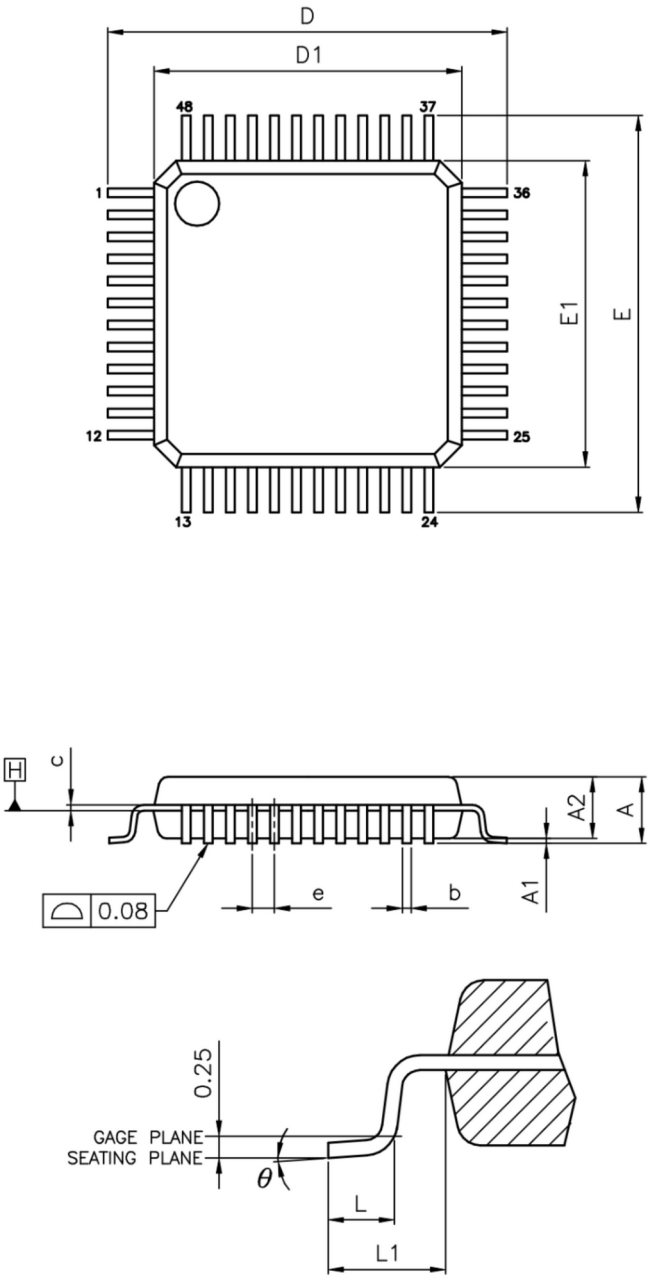
Functional TNOW Timing

Idle/receive: TNOW low. Before the first start bit: TNOW becomes high. During start, data, optional parity and stop bits: TNOW remains high. After the final stop bit is fully transmitted: TNOW returns low. This sequence is functional and not a characterized nanosecond timing specification.

10. Package Information

10.1 LQFP48 Mechanical Drawing

Figure 7. LQFP48 7 mm x 7 mm package mechanical drawing (top, side and lead detail views).



PACKAGE DEFINITION: The package has 48 leads and no exposed pad. Dimensions are in millimetres. The drawing is not to scale.

10. Package Information (continued)

10.2 Mechanical Dimensions

Table 35. LQFP48 package dimensions

Symbol	Description	Minimum	Typical	Maximum	Unit
A	Overall package height	-	-	1.60	mm
A1	Standoff	0.05	-	0.15	mm
A2	Body thickness	1.35	1.40	1.45	mm
b	Lead width	0.17	0.22	0.27	mm
c	Lead thickness	0.09	-	0.20	mm
D	Overall horizontal span	8.80	9.00	9.20	mm
D1	Molded body width	6.90	7.00	7.10	mm
E	Overall vertical span	8.80	9.00	9.20	mm
E1	Molded body length	6.90	7.00	7.10	mm
e	Lead pitch	-	0.50 BSC	-	mm
θ	Lead angle	0°	3.5°	7°	degree
L	Lead length	0.45	0.60	0.75	mm
L1	Lead reference length	-	1.00 REF	-	mm

The 0.08 mm geometric callout in Figure 7 is the maximum lead coplanarity/profile limit.

10.3 Thermal Reference

Junction-to-ambient thermal resistance is 87.4 °C/W for the LQFP48 package, based on a simulated 1.6 mm, two-layer glass-epoxy board. Under that reference model, the thermal design limit at TA = +105 °C and TJ = +125 °C is 229 mW. These are package/board thermal limits, not measured XL1326 operating power. Both depend on copper area, airflow, component placement and PCB construction.

10.4 PCB Footprint Boundary

Figure 7 defines package geometry only and is not a solder-land pattern. Use a validated LQFP48 7 mm x 7 mm, 0.50 mm-pitch footprint and confirm copper, solder-mask and paste dimensions with the selected assembly process.

10.5 Assembly, Packaging and Compliance

The current controlled packaging and compliance statement is provided with the applicable order or production lot.

11. Ordering and Marking

11.1 Ordering Information

Table 36. Ordering information

Orderable code	Package	Temperature range	Status
XL1326-LQ48	LQFP48, 7 mm x 7 mm, 0.50 mm pitch	-40 °C to +105 °C	Production

11.2 Top Marking

Table 37. Top marking legend

Line	Content
1	XILUME brand identifier
2	Device code XL1326
3	Date and traceability code; exact format may vary by production lot

11.3 Related Documentation

Section 6 defines the device-level host protocol. Platform-specific driver packages, API documentation, release notes and test utilities are maintained as separate integration documents so the XL1326 device specification remains independent of any one host product or operating system.

Important Notice

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